

F1C26

Specification and Datasheet

Confidential / Preliminary Documentation

Revision 1.5

F1media Co., Ltd.

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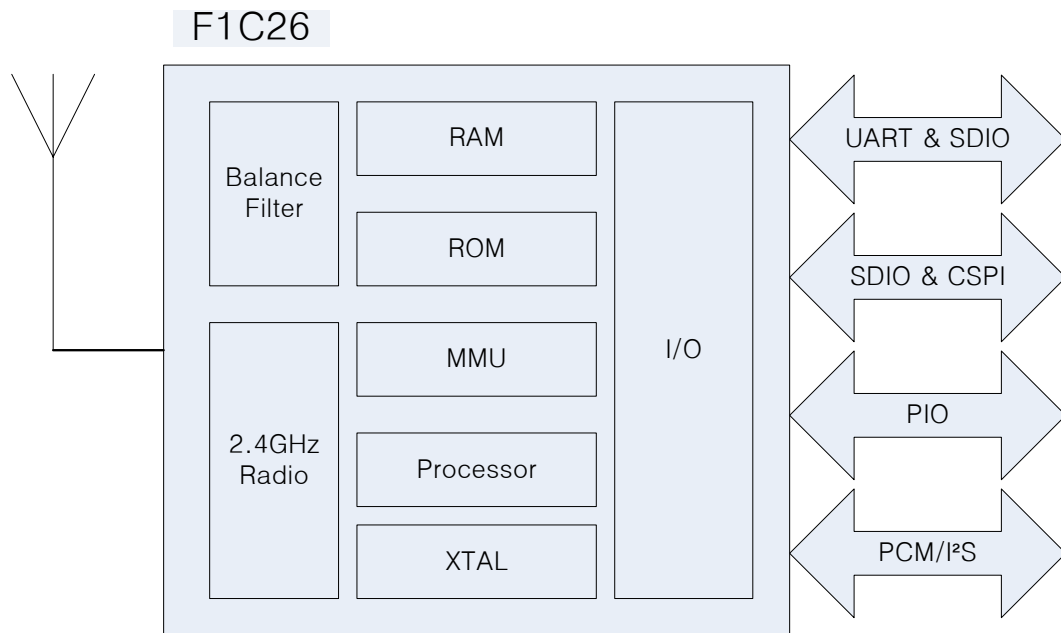
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1. General

1.1 Overview

This specification covers Bluetooth module (class-2) which complies with Bluetooth specification version 2.1 + EDR and integrates RF & Baseband controller in small package. This Module has deployed CSR's BC06-ROM WLCSP chipset.



1.2 Features

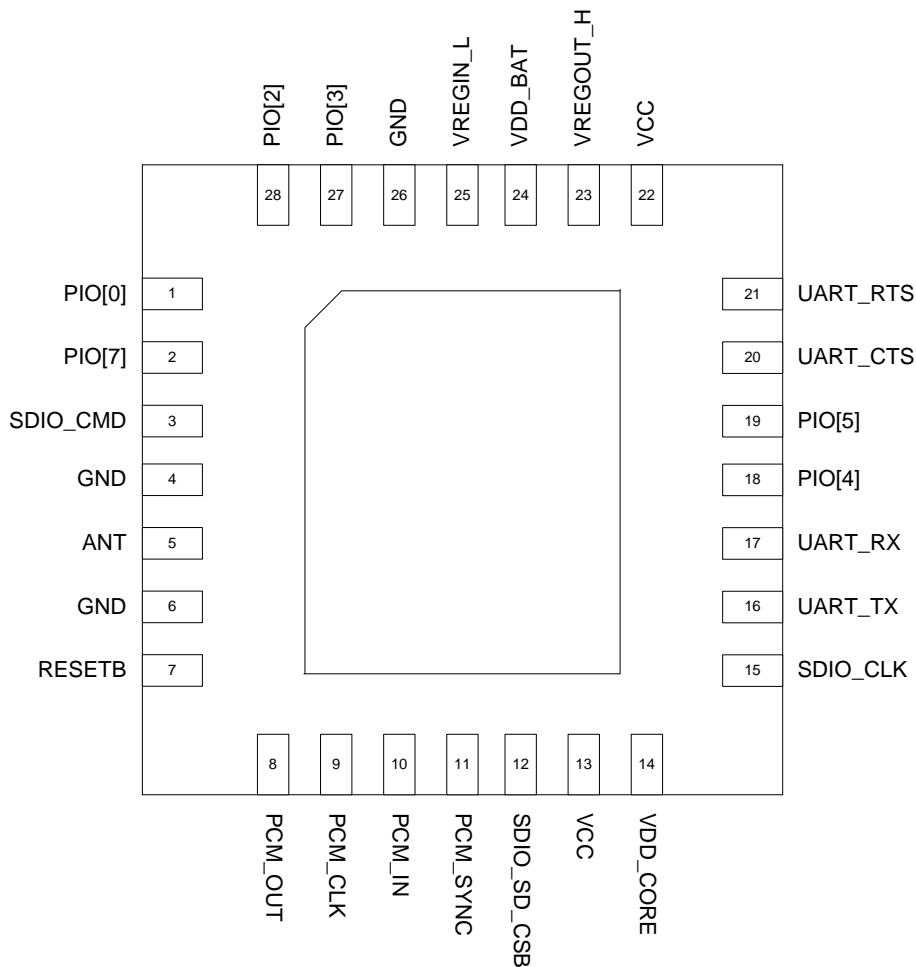
- Fully Qualified Bluetooth v2.1 + EDR System
- Enhanced Data Rate (EDR) compliant with v2.1 of specification for both 2Mbps and 3Mbps modulation modes
- Full-speed Bluetooth Operation with Full piconet Support (Up to 7 Slaves)
- Scatternet Support
- Ultra Low Power Consumption
- Excellent Compatibility with Cellular Telephones
- Support for 802.11 Co-existence
- Integrated transcoders for A-law, u-law and linear PCM
- UART, SDIO, CSPI interface by setting
- Flexible Supply Voltage : 1.8V supply or 2.7~3.3V range supply

- Standard HCI support
- Integrated 4Mbit ROM
- Integrated 26MHz Reference Clock
- Competitive Size : 8mm x 7mm x 1.5mm (W x L x H, with CAN)

1.3 Application

- Cellular Handsets
- Personal Digital Assistants (PDA)
- Space critical application
- Digital Cameras and other high-volume consumer product

1.4 Pinout Diagram & Outline Size

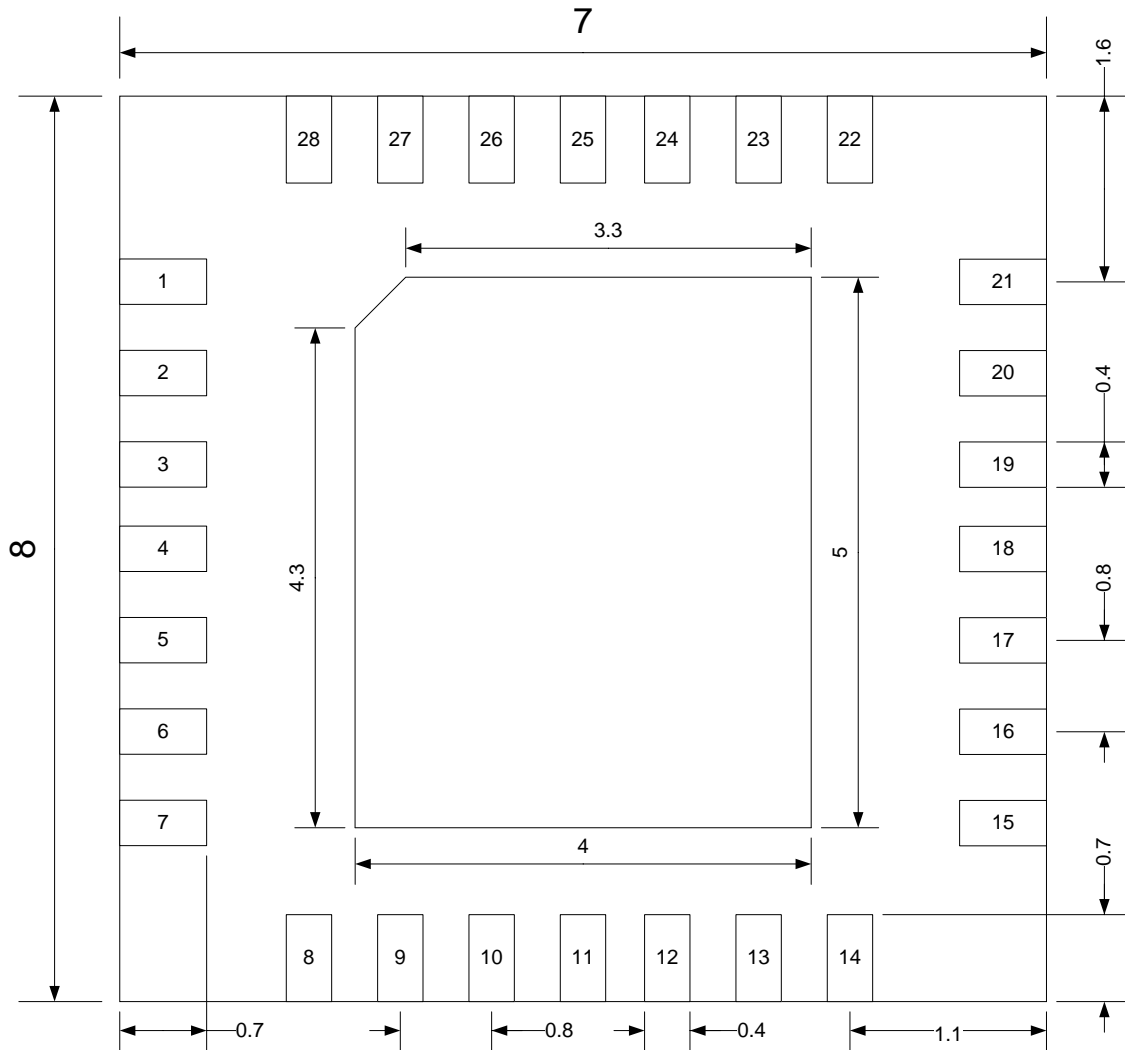


1.5 Device Terminal Functions

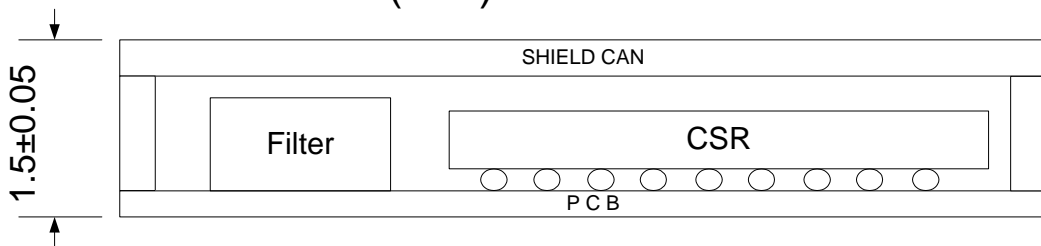
	PIN	Name	Description
PCM	PCM_OUT	8	Synchronous data output
	PCM_IN	10	Synchronous data input
	PCM_CLK	9	Synchronous data clock
	PCM_SYNC	11	Synchronous data sync
UART	UART_RTS	21	UART request to send, active low
	UART_TX	16	UART data output, active low
	UART_CTS	20	UART clear to send, active low
	UART_RX	17	UART data input, active low (idle status high)
SDIO	SDIO_CLK	15	SDIO Clock
	SODI_SD_CSB	12	SDIO chip select
	SDIO_CMD	3	SDIO data input
	SDIO_DATA0	16	SDIO synchronous data input/output
	SDIO_DATA1	21	SDIO synchronous data input/output
	SDIO_DATA2	17	SDIO synchronous data input/output
PIO	SDIO_DATA3	20	SDIO synchronous data input/output
	PIO[0]	1	Programmable input/output line
	PIO[2]	28	Programmable input/output line
	PIO[3]	27	Programmable input/output line
	PIO[4]	18	Programmable input/output line
	PIO[5]	19	Programmable input/output line
	PIO[7]	2	Programmable input/output line
Other Pins	ANT	5	RF Connection to Antenna
	GND	4,6,26	Ground
	VCC	13,22	Main supply input voltage. Regulated DC Source recommended
	VDD_CORE	14	Power supply for internal digital circuitry
	VREGIN_L	25	Input to internal low-voltage regulator
	VREGOUT_H	23	Input to internal low-voltage regulator
	VDD_BAT	24	High-voltage regulator output
	RESETB	7	Input to internal high-voltage regulator Reset if low.

1.6 Module Dimension

1. Top View (mm)



2. Side View (mm)



2. Characteristics

2.1 Electrical Characteristics

Absolute Maximum Ratings		
Rating	MIN	MAX
Storage temperature	-40°C	85°C
Supply voltage : VCC (CASE 1)	-0.4V	3.7V
Supply voltage : VCC (CASE 2)	-0.4V	2.7V
Other terminal voltages	VSS-0.4V	VCC+0.4V

Recommended Operating Conditions		
Operating Condition	MIN	MAX
Operating temperature range	-30°C	85°C
Supply voltage : VCC (CASE 1)	2.7V	3.3V
Supply voltage : VCC (CASE 2)	1.7V	1.9V

2.2 RF Characteristics

Transmitter

Specification	Condition	MIN	TYP	MAX	UNIT
Output transmit power	Normal	-6	1	4	dBm
Transmit power density	Normal			4	dBm
Transmit power control	Normal	2		8	dBm
Frequency Range	Normal	2400		2483.5	MHz
20dB bandwidth for modulated carrier	Normal		850	1000	KHz
Adjacent channel transmit power	±2MHz ±3MHz ±4MHz			-20 -40 -40	dBm
Modulation Characteristics	f1avg	140		175	KHz
	f2max	115			KHz

	f2avg / f1avg			80	%
Initial carrier frequency tolerance	Normal	-20		20	KHz
Carrier frequency Drift	One slot packet(DH1)	-25		25	KHz
	Three slot packet(DH3)	-40		40	
	Five slot packet(DH5)	-40		40	

Transceiver

Specification	Condition	MIN	TYP	MAX	UNIT
Adjacent channel transmit power	30MHz ~ 1GHz			-36	dBm
	1GHz ~12.75GHz			-30	
	1.8GHz ~5.1GHz			-47	
	5.1GHz ~5.3GHz			-47	

Receiver

Specification	Condition	MIN	TYP	MAX	UNIT
Sensitivity level (0.1% BER)	Single slot packets	-70	-78		dBm
Transmit power density	Multi slot packet	-70	-78		dBm
C/I performance	co-channel 1MHz (Adjacent channel)			11 0	dB
	2MHz (2nd Adjacent channel)			-30	
	3MHz (3rd Adjacent channel)			-40	
Blocking performance	30MHz ~ 2000MHz	-10			dBm
	2000MHz ~ 2400MHz	-27			
	2500MHz ~ 3000MHz	-27			
	3000MHz ~ 12.75GHz	-10			
Intermodulation performance	n=5	-39			dBm
Maximum input level		-20	-10		dBm

3. Interface

3.1 HOST Selection

F1C26 Module switches between UART and SDIO transport at boot-up by reading the status of PIO[4]:

- PIO[4] = pulled low: UART mode is selected.
- PIO[4] = driven high: SDIO or CSPI host interface is selected.

The protocol used by the UART host interface is determined by the status of the SDIO_CLK and SDIO_CMD lines at the time PIO[4] is sampled. Table 3.1 lists the different protocols available along with the required configuration of CLK and CMD for each one. To select a different UART Protocol, connect external 100kΩ pull-up and/or pull-down resistors as appropriate.

For example:

- To select BCSP, connect 100kΩ pull-downs to both SDIO_CLK and SDIO_CMD.
- To select H4DS, connect a 100kΩ pull-up to SDIO_CLK and a 100kΩ pull-down to SDIO_CMD.

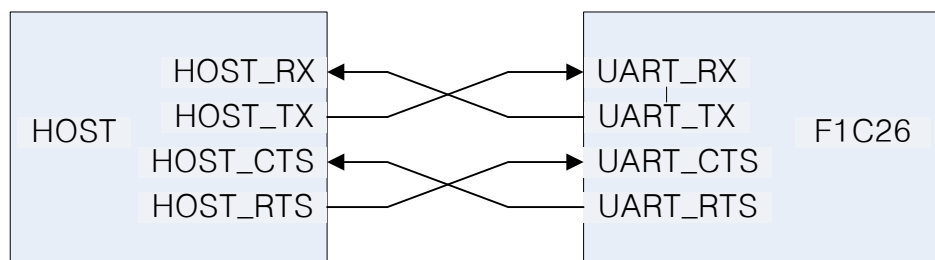
CLK	CMD	UART Protocol
0	0	BCSP
0	1	H4
1	0	H4DS
1	1	H5

< Table3.1 UART Protocol Selection >

3.2 UART interface

Four signals are used to implement the UART function.

UART_TX and UART_RX transfer data between the two devices. The remaining two signals, UART_CTS and UART_RTS, can be used to implement RS232 hardware flow control where both are active low indicators.



3.2.1 UART Setting

User can change data format the following selection using PSKEY.

However, host shall communicate with default setting UART connection initiated at first time.

$$\text{Baud Rate} = (\text{PSKEY_UART_BAUD_RATE}) / 0.004096$$

Parameter	Possible value
Baud Rate	9600 ~ 3M Baud
Flow Control	None
Parity	None, Odd or Even
Number of Stop Bits	1 or 2
Bits per channel	8

3.3 SDIO

F1C26 selects UART/SDIO interface by reading PIO[4] at boot-time. When PIO[4] is high, the SDIO interface is enabled. When PIO[4] is low, the UART is enable. When SDIO mode, F1C26 provides all defined slave modes, but not SD host function. For more information, see the following specifications.

- SD Specifications Part 1 Physical layer specification v1.10
- SD Specifications Part E1 SDIO specification v1.10
- SDIO Card Part E2 Type-A Specification for Bluetooth v1.00

3.4 PCM

Pulse Code Modulation (PCM) is a standard method used to digitize audio (particularly voice) patterns for transmission over digital communication channels. Through its PCM interface, this module has hardware support for continual transmission and reception of PCM data, so reducing processor overhead for wireless headset applications. This module offers a bi-directional digital audio interface that route directly into the baseband lauer of the on-chip firmware. It dose not pass through the HCI protocol layer.

Hardware allows the data to be sent to and received from a SCO connection. This module interfaces directly to PCM audio devices including the following:

- Qualcomm MSM 3000 series and MSM 5000 series CDMA baseband devices
- OKI MSM7705 for channel A-law and u-law CODEC
- Motorola MC145481 8-bit A-law and u-law CODEC
- Motorola MC145483 13-bit linear CODEC
- STW 5093 and 5094 14-bit linear CODECs

3.4.1 PCM Configuration

The PCM configuration is set using two PS keys, PSKEY_PCM_CONFIG32 and PSKEY_PCM_LOW_JITTER_CONFIG. The default for long frame sync and interface master generating 256KHz PCM_CLK with no tri-stating of PCM_OUT.

Parameter	Possible value
Mode	Slave, Master
Clock rate	Master Mode : 128, 256, 512KHz Slave Mode : up to 2048KHz
Sync formats	Long frame sync, Short frame sync
Data formats	13 or 16bit linear, 8-bit A-law to u-law

3.4.2 Digital Audio Interface (I²S)

The digital audio interface supports the industry standard formats for I²S, left-justified or right-justified.

The interface shares the same pins as the PCM interface, which means each audio bus is mutually exclusive in its usage.

PCM Interface	I ² S Interface
PCM_OUT	SD_OUT
PCM_IN	SD_IN
PCM_SYNC	WS
PCM_CLK	SCK

Table describes the values for the PS Key PSKEY_DIGITAL_AUDIO_CONFIG that is used to set-up the digital audio interface. For example, to configure an I2S interface with 16-bit SD data set PSKEY_DIGITAL_AUDIO_CONFIG to 0x0406.

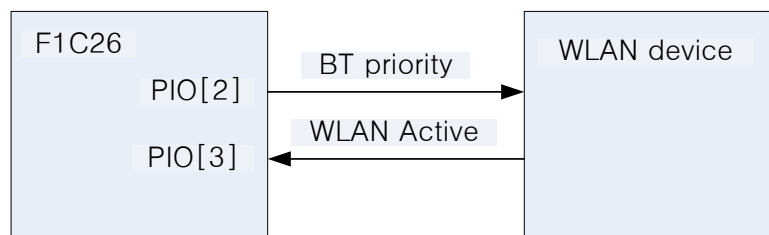
Bit	Mask	Name	Description
D[0]	0x0001	CONFIG_JUSTIFY_FORMAT	0: left justified. 1: right justified.
D[1]	0x0002	CONFIG_LEFT_JUSTIFY_DELAY	For left justified formats: <ul style="list-style-type: none"> ■ 0: is MSB of SD data occurs in the first SCLK period following WS transition ■ 1: is MSB of SD data occurs in the second SCLK period.

D[2]	0x0004	CONFIG_CHANNEL_POLARITY	0: SD data is left channel when WS is high. 1: SD data is right channel.
D[3]	0x0008	CONFIG_AUDIO_ATTEN_EN	0: 17-bit SD data is rounded down to 16bits. 1: the audio attenuation defined in CONFIG_AUDIO_ATTEN is applied over 24 bits with saturated rounding. Requires CONFIG_16_BIT_CROP_EN to be 0.
D[7:4]	0x00f0	CONFIG_AUDIO_ATTEN	Attenuation in 6dB steps.
D[9:8]	0x0300	CONFIG_JUSTIFY_RESOLUTION	Resolution of data on SD_IN: <ul style="list-style-type: none"> ■ 00: 16-bit ■ 01: 20-bit ■ 10: 24-bit ■ 11: reserved This is required for right justified format and with left justified LSB first.
D[10]	0x0400	CONFIG_16_BIT_CROP_EN	0: 17-bit SD_IN data is rounded down to 16bits. 1: only the most significant 16bits of data are received.

< Table : PSKEY_DIGITAL_AUDIO_CONFIG >

3.5 Co-existence with WLAN

3.5.1 2-wire Co-existence

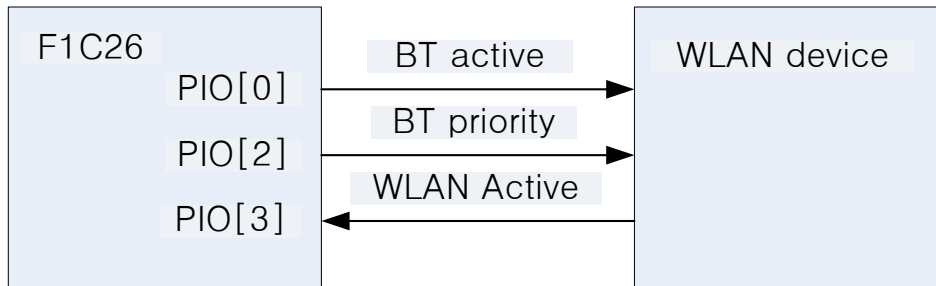


High priority BT packet is protected. WLAN must cancel or abort all transmissions immediately while BT priority is generated, apart from those transmissions required to maintain the link to AP.

PSkey setting is below

- BT priority
 PSSET 0x0246 0x0000
 PSSET 0x0029 0x0004 0x0000
- WLAN active
 PSSET 0x0028 0x0008 0x0000 0x0000

3.5.2 3-wire Co-existence Traditional

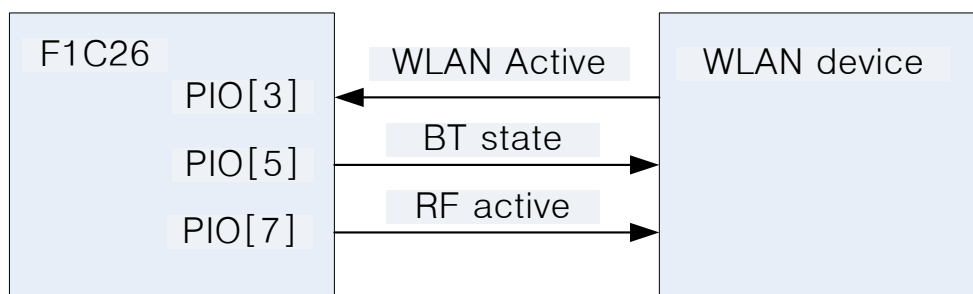


The traditional 3-wire co-existence is the same as the 2-wire, with the addition of BT active.

PSkey setting is below

- BT priority
PSSET 0x0246 0x0000
PSSET 0x0029 0x0004 0x0000
- BT active
PSSET 0x0209 0x01
PSSET 0x03b0 0x00
PSSET 0x0031 0x0000 0x0001 0x0000 0x0000 0x0800
- WLAN active
PSSET 0x0028 0x0008 0x0000 0x0000

3.5.3 3-wire Co-existence Enhanced



The enhanced 3-wire co-existence is the same as the traditional 3-wire. But the timing diagram for the enhanced method are more complex and contain more information regarding the transaction.

PSkey setting is below

- BT state, BT active
PSSET 0x002a 0x11
- WLAN active
PSSET 0x0028 0x0008 0x0000 0x0000

3.6 Reset

F1C26 may be reset from several sources.

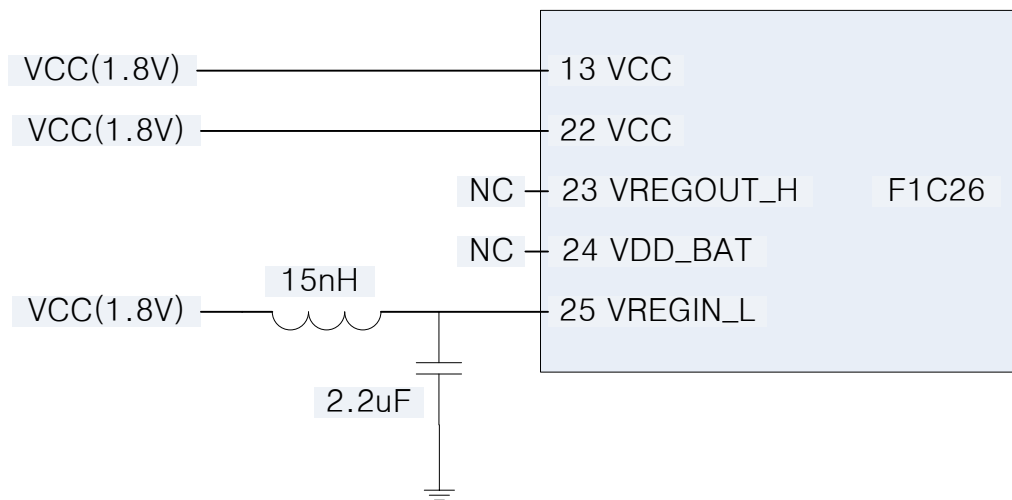
- RESETB
- Power on reset
- UART break character or via a software configured watchdog timer.

The hardware reset is performed at low reset. The reset will be performed 1.5ms and 4.0ms following RESETB being active low. The reset must be in high state for normal operation.

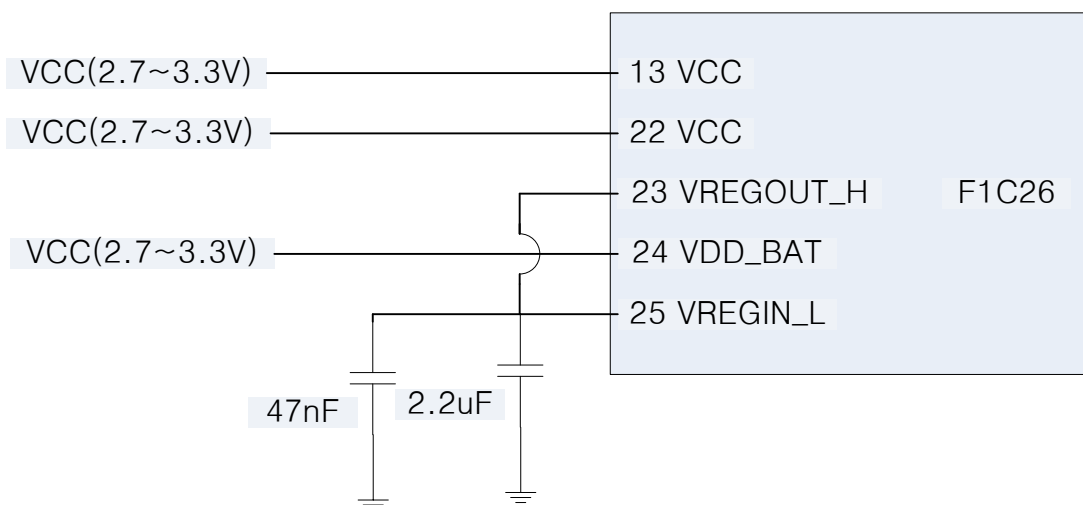
4. Power Supply Voltage

There are two method for supply voltage. 1.8V and 2.7~3.3V.

4.1 1.8V Supply



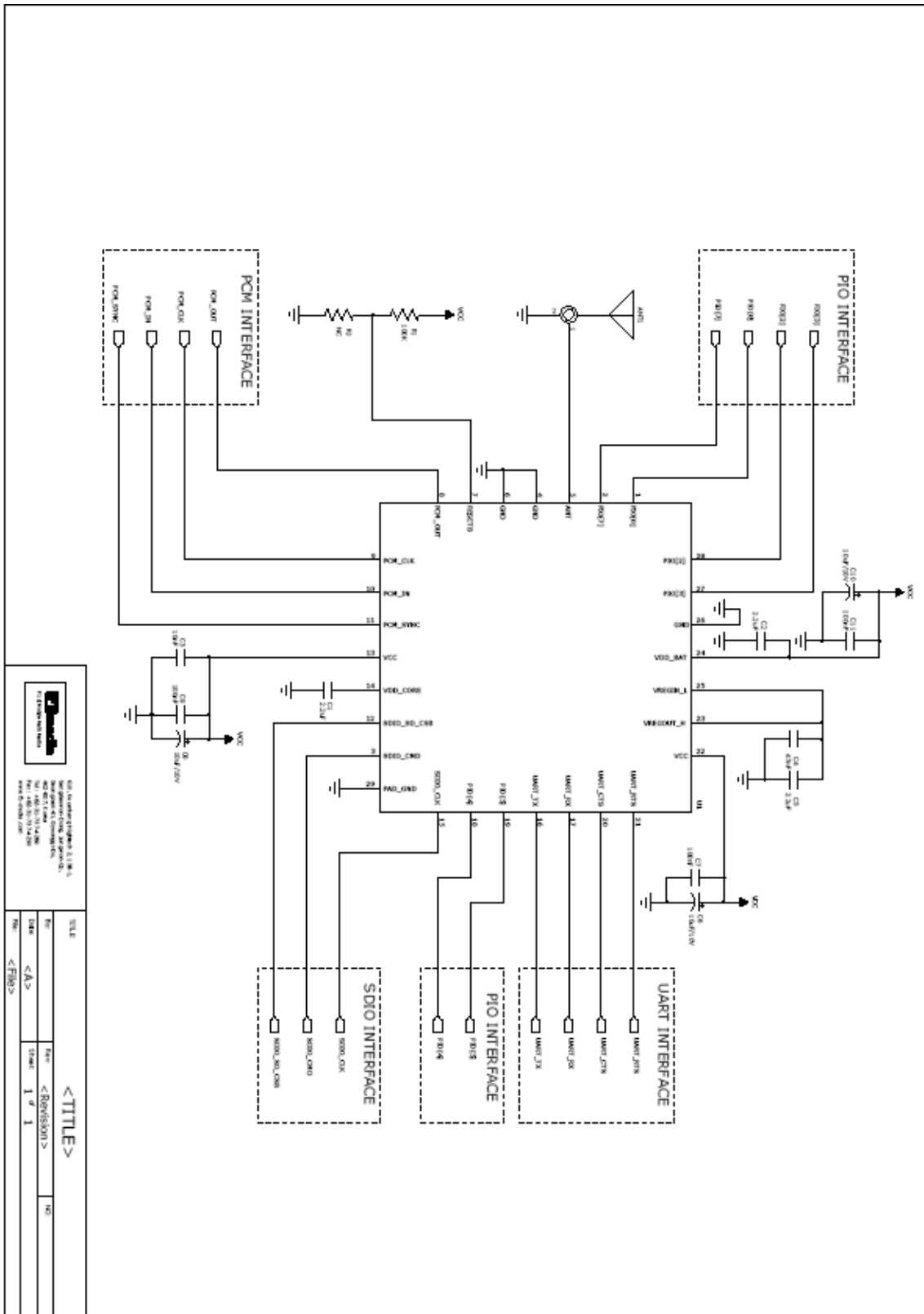
4.2 2.7~3.3V Supply



5.2 2.7~3.3V Supply

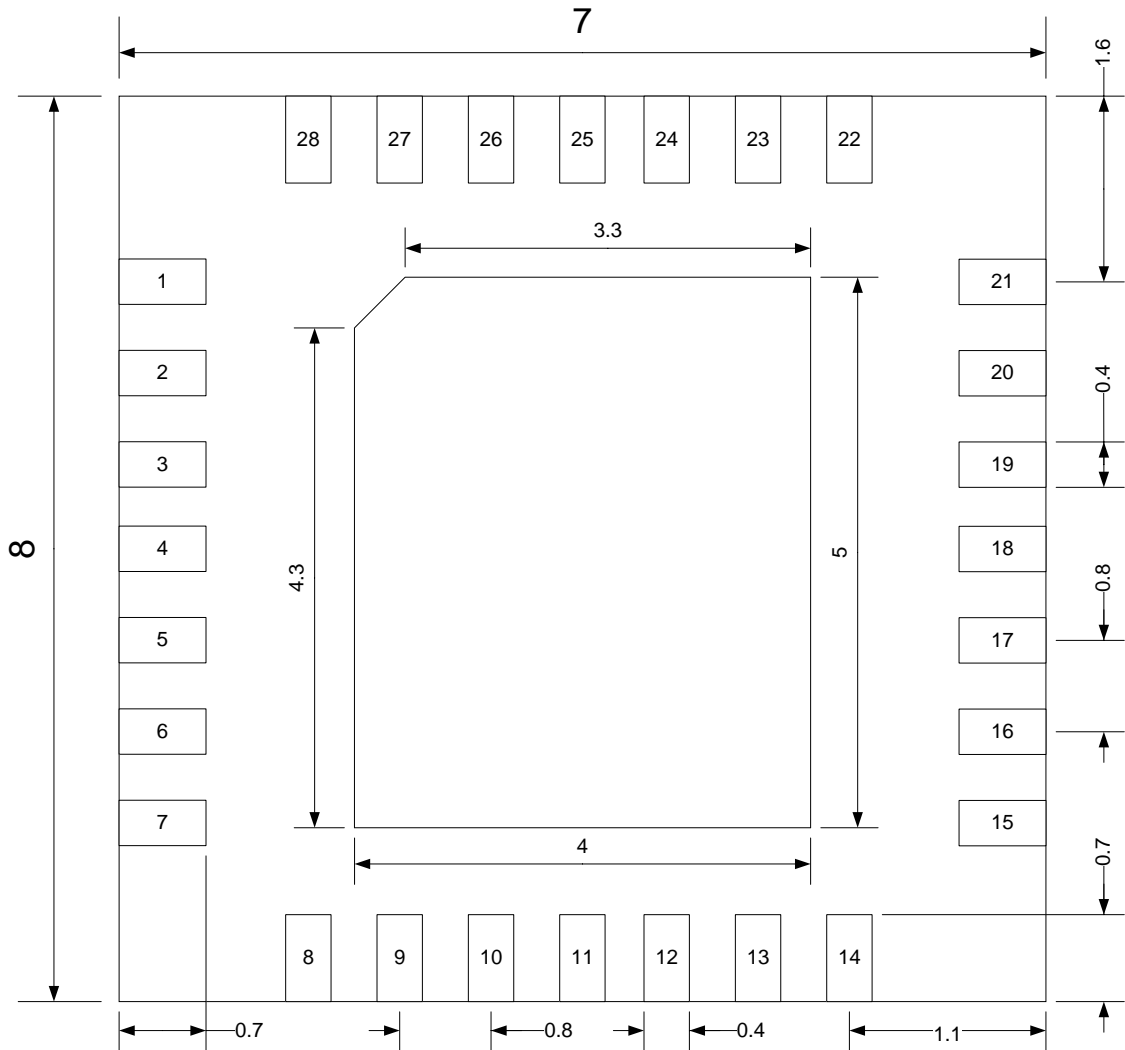
[SCH]F1C26_REV
A1.0(INPUT VOLT.)

[SCH]F1C26_REV
A1.0(INPUT VOLT.)

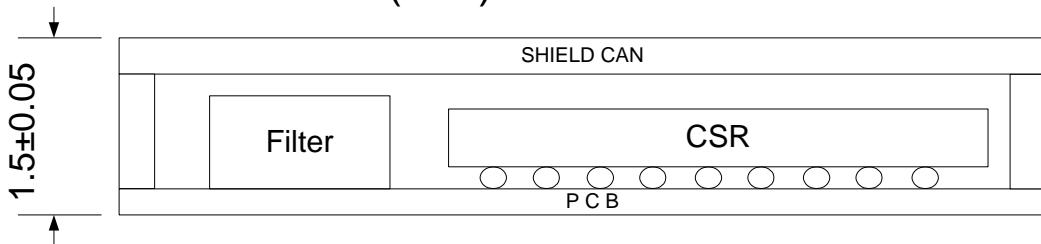


6. Dimension

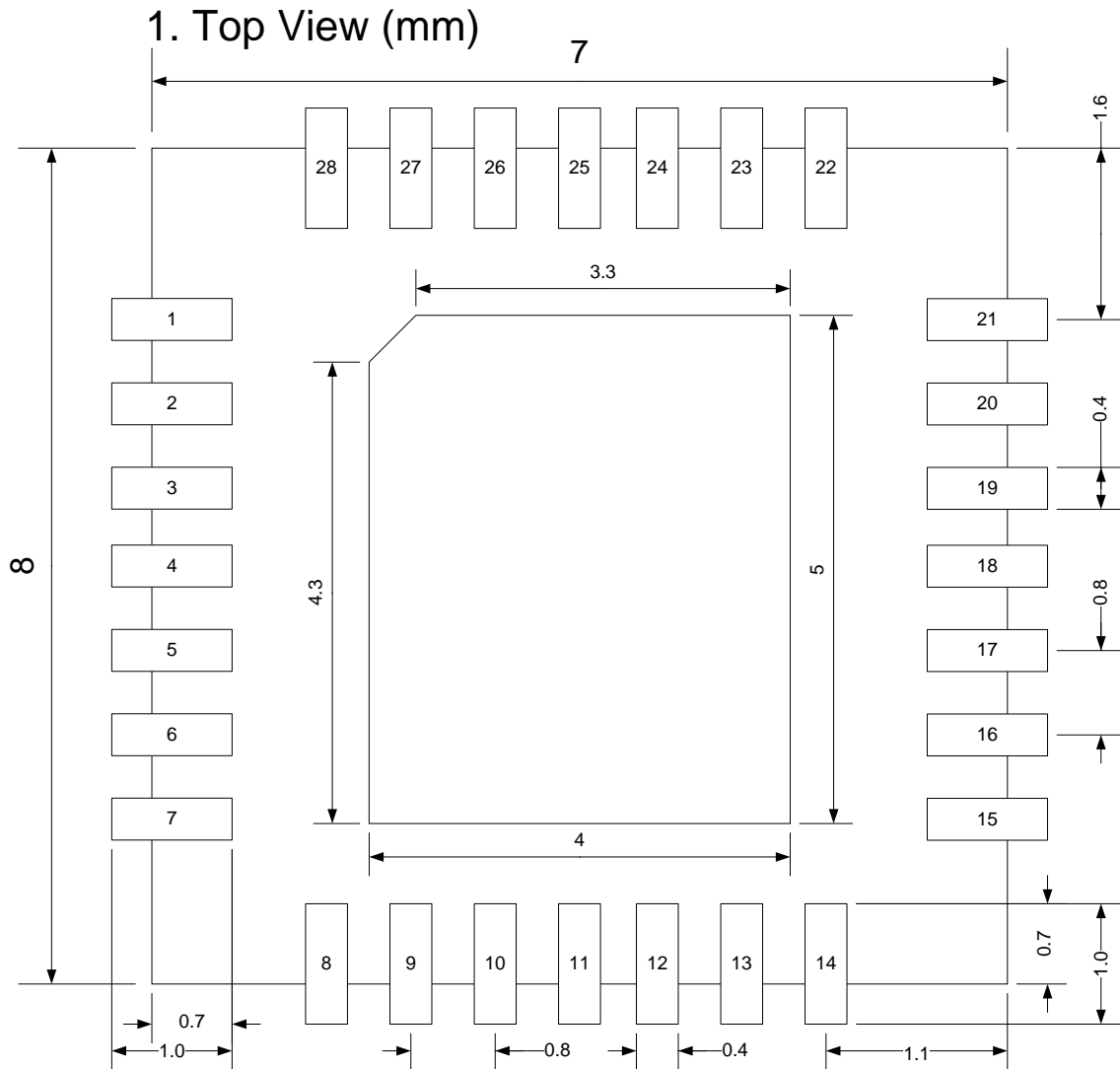
1. Top View (mm)



2. Side View (mm)

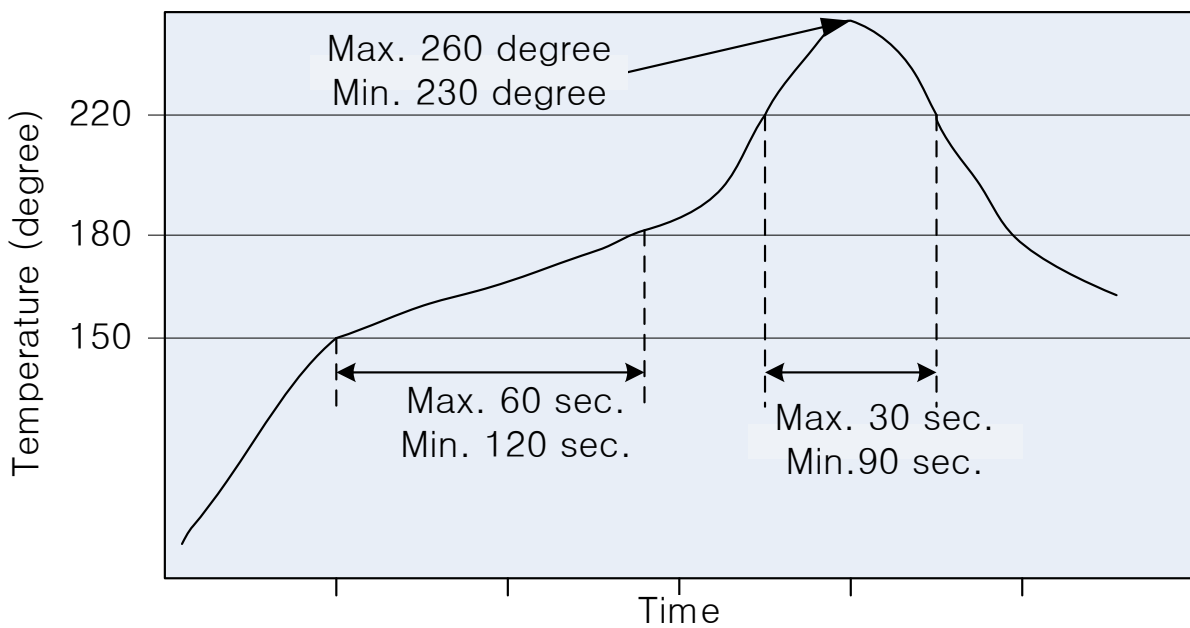


7. PCB Layout



8. Reflow Temperature Profile

Recommended solder reflow profile are shown in below and follow the lead-free profile in accordance with JEDEC Std 20C. Table lists the critical reflow temperatures. Flux residue remaining from board assembly can contribute to electrochemical migration (ECM) over time. This depends on a number of factors, including flux type, amount of flux residue remaining after reflow, and stress conditions during product use, such as temperature, humidity, and potential difference between pins. Care should be taken in selecting production board/module assembly processes and materials, taking into account these factors.



Process Step	Lead-Free Solder
Ramp rate	3°C/sec
Preheat	Max. 150°C to 180°C, 60 to 180 sec
Time above liquids	+220°C 30 to 90 sec
Peak temperature	+255°C ±5°C
Time within 5°C of peak temperature	10 to 20 sec
Ramp-down rate	6°C/sec max

9. Revision History

Revision	Date	Change Descriptions	Issued by
Rev 1.0	2010-03-23	Initial release	S.J.LEE
Rev 1.1	2010-05-25	Dimension data update	H.G.SEO
Rev 1.2	2011-02-14	Operating Temperature Revision	J.M.KWON
Rev 1.3	2011-03-02	Storage Temperature Revision	J.M.KWON
Rev 1.4	2011-04-15	Audio Interface Revision	J.M.KWON
Rev 1.5	2012-01-10	Height Update	J.M.KWON