

F1C23

Databook

Confidential / Preliminary Documentation

Revision 1.4

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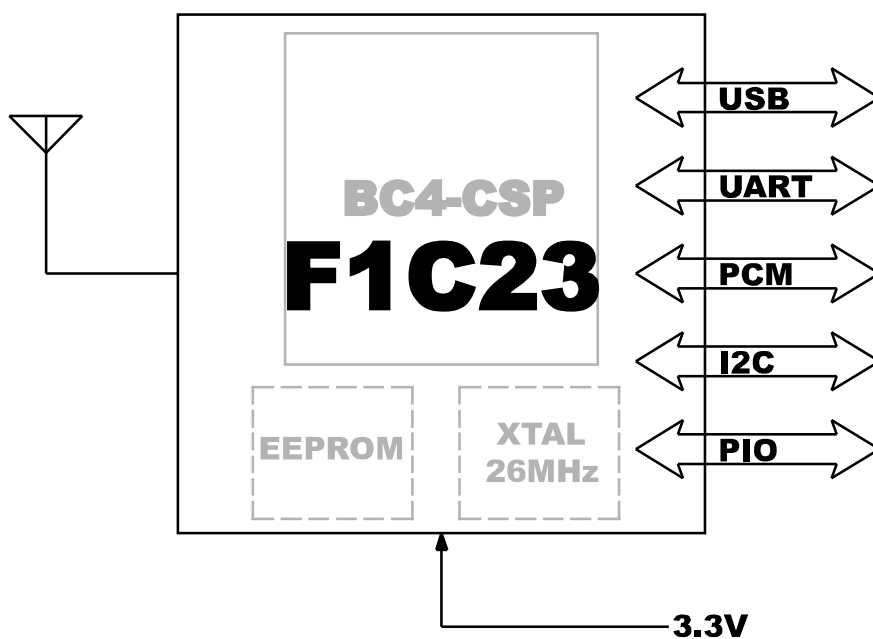
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1. General

1.1 overview

This specification covers Bluetooth module (class-2) which complies with Bluetooth specification version 2.0 + EDR and integrates RF & Baseband controller in small package. This Module has deployed CSR's BC04-ROM CSP EDR chipset.

All detailed specification including pinouts and electrical specification may be changed without notice.



Overview F1C23

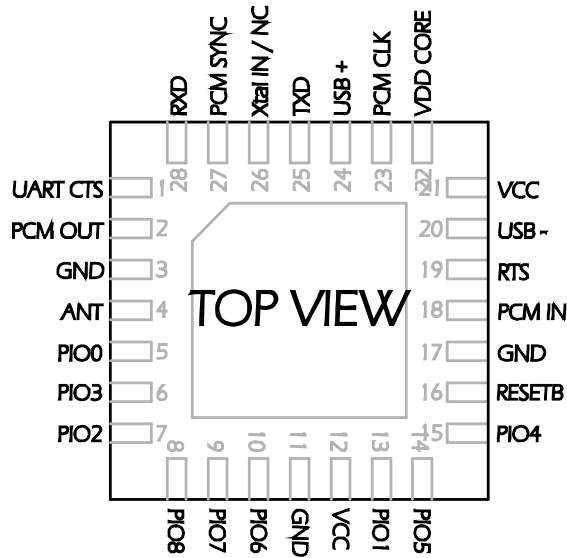
1.2 Features

- Fully Qualified Bluetooth v2.0 + EDR System
- Enhanced Data Rate (EDR) compliant with v2.0.e.2 of specification for both 2Mbps and 3Mbps modulation modes
- Full-speed Bluetooth Operation with Full Piconet Support
- Scatternet Support
- Ultra Low Power Consumption
- Excellent Compatibility with Cellular Telephones
- Support for 802.11 Co-existence
- RoHS Compliant
- Integrated transcoders for A-law, u-law and linear PCM
- UART interface with programmable baud rate up to 3Mbits/s with an optional bypass mode
- Full-speed USB v2.0 interface supports OHCI and UHCI host interface
- Standard HCI (UART and USB) support
- Integrated 4Mbit ROM & 48Kbyte RAM
- Integrated 26MHz Reference Clock (Option)
- Integrated 16Kbit EEPROM (Option)
- Competitive Size (6mm x 6mm x 1.06mm : QFN 28Pin)

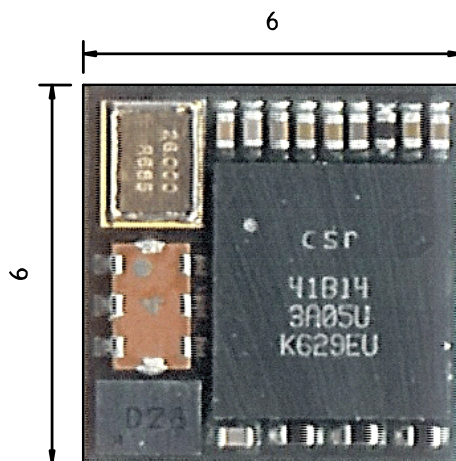
1.3 Application

- Cellular Handsets
- Personal Digital Assistants (PDA)
- Space critical application
- Digital Cameras and other high-volume consumer product
- USB Dongle

1.4 Pinout Diagram & Outline Size



F1C23 Pinout Diagram

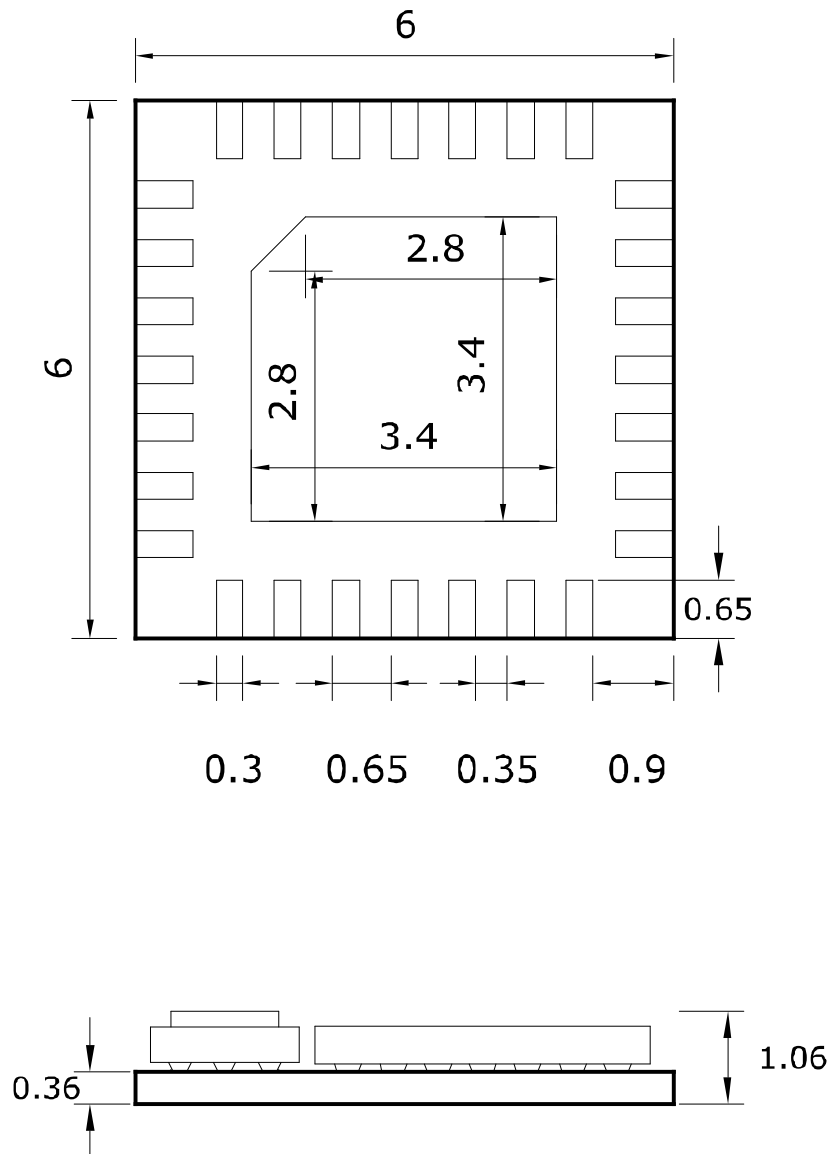


F1C23 Outline Size

1.5 Device Terminal Functions

	PIN	Name	Description
PCM	PCM OUT	2	Synchronous data output
	PCM IN	18	Synchronous data input
	PCM CLK	23	Synchronous data clock
	PCM SYNC	27	Synchronous data sync
UART	RTS	19	UART request to send, active low
	TXD	25	UART data output, active low
	CTS	1	UART clear to send, active low
	RXD	28	UART data input, active low (idle status high)
USB	USB -	20	USB -
	USB +	24	USB + with selectable internal 1.5k pull-up resistor
PIO & AIO	PIO0	5	Programmable input/output line PIO 6,7,8 Can be used to form I2C interface
	PIO1	13	
	PIO2	7	
	PIO3	6	
	PIO4	15	
	PIO5	14	
	PIO6	10	
	PIO7	9	
	PIO8	8	
Other Pins	ANT	4	RF Connection to Antenna
	GND	3,11,17	Ground
	VCC	12,21	Main supply input voltage. Regulated DC Source recommended
	VDD CORE	22	D.C Input voltage for operation of Core and RF block (1.7~1.9V)
	Xtal IN / NC	26	Xtal IN / NC. <u>Do not connect NC to GND</u>
	RESETB	16	Reset if low. Input debounced so must be low for >5ms to cause a reset

1.6 Module Dimension



2. Characteristics

2.1 Electrical Characteristics

Absolute Maximum Ratings		
Rating	Minimum	Maximum
Storage temperature	-40°C	85°C
Supply voltage : VCC	-0.4V	3.7V
Supply voltage : VDD_CORE	-0.4V	2.2V
Other terminal voltages	VSS-0.4V	VCC+0.4V

Recommended Operating Conditions			
Operating Condition		Minimum	Maximum
Operating temperature range	A	-20°C	70°C
	B	-30°C	85°C
	C	-40°C	85°C
Supply voltage : VCC		1.7V	3.6V
Supply voltage : VDD_CORE		1.7V	1.9V

2.2 RF Characteristics

Transmitter

Specification	Condition	Min	Typ	Max	Unit
Output transmit power	Normal	-6	1	4	dBm
Transmit power density	Normal			4	dBm
Transmit power control	Normal	2		8	dBm
Frequency Range	Normal	2400		2483.5	MHz
20dB bandwidth for modulated carrier	Normal		850	1000	KHz
Adjacent channel transmit power	±2MHz ±3MHz ±4MHz			-20 -40 -40	dBm
Modulation Characteristics	f1avg f2max f2avg / f1avg	140 115		175 80	KHz KHz %
Initial carrier frequency tolerance	Normal	-20		20	KHz
Carrier frequency Drift	One slot packet(DH1) Three slot packet(DH3) Five slot packet(DH5)	-25 -40 -40		25 40 40	KHz

Transceiver

Specification	Condition	Min	Typ	Max	Unit
Adjacent channel transmit power	30MHz ~ 1GHz 1GHz ~12.75GHz 1.8GHz ~5.1GHz 5.1GHz ~5.3GHz			-36 -30 -47 -47	dBm

Receiver

Specification	Condition	Min	Typ	Max	Unit
Sensitivity level (0.1% BER)	Single slot packets	-70	-78		dBm
Transmit power density	Multi slot packet	-70	-78		dBm
C/I performance	co-channel 1MHz (Adjacent channel) 2MHz (2nd Adjacent channel) 3MHz (3rd Adjacent channel)			11 0 -30 -40	dB
Blocking performance	30MHz ~ 2000MHz 2000MHz ~ 2400MHz 2500MHz ~ 3000MHz 3000MHz ~ 12.75GHz	-10 -27 -27 -10			dBm
Intermodulation performance	n=5	-39			dBm
Maximum input level		-20	-10		dBm

3. Terminal Description

3.1 UART

Four signals are used to implement the UART function.

UART_TXD and UART_RXD transfer data between the two devices. The remaining two signals, UART_CTS and UART_RTS, can be used to implement RS232 hardware flow control where both are active low indicators.

3.1.1 UART Setting

User can change data format the following selection using PSKEY.

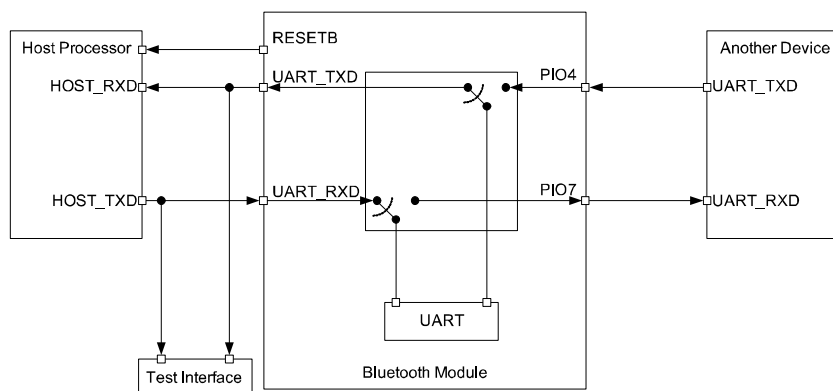
However, host shall communicate with default setting UART connection initiated at first time.

$$\text{Baud Rate} = (\text{PSKEY_UART_BAUD_RATE}) / 0.004096$$

Parameter	Possible value
Baud Rate	9600 ~ 3M Baud
Flow Control	None
Parity	None, Odd or Even
Number of Stop Bits	1 or 2
Bits per channel	8

3.1.2 UART Bypass Mode

switch the bypass to PIO4, 7 as shown in figure. When the bypass mode has been invoked, module enters the deep sleep state indefinitely



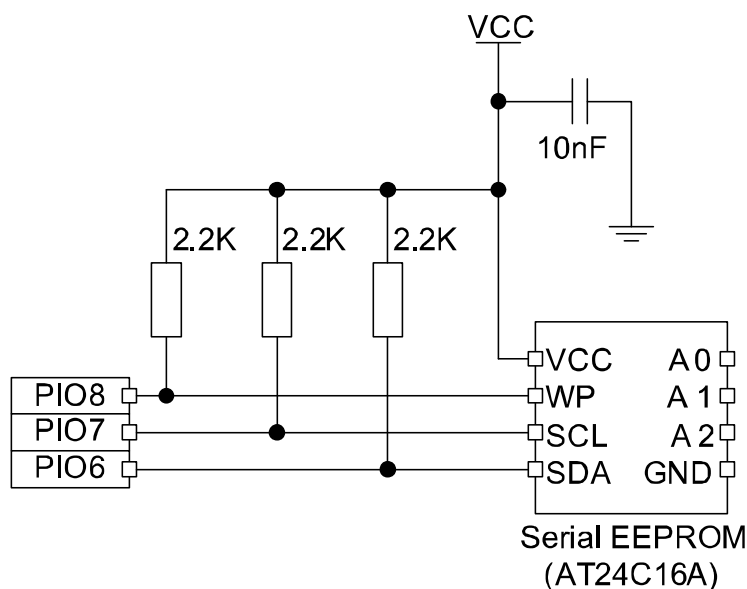
3.2 USB

This Bluetooth module contains a full speed (12Mbit/s) USB interface that is capable of driving a USB cable directly. No external USB transceiver is required. The device operates as a USB peripheral, responding to requests from a master host controller such as a PC. Both the OHCI and the UHCI standards are supported. The set of USB endpoints implemented can behave as specified in the USB section of the Bluetooth specification v2.0 + EDR or alternatively can appear as a set of endpoints appropriate to USB audio devices such as a set of USB speakers. USB is a master/slave oriented system (in common with other USB peripherals). This Module only supports USB slave operation.

3.3 I²C

PIO[8:6] can be used to form an interface. The interface is driven by “bit banging” these PIO pins using software. Therefore it is suited only to relatively slow functions such as driving a dot matrix liquid crystal display (LCD).

Note. PIO[7:6] dual functions, UART bypass and EEPROM support, therefore devices using an EEPROM connect support UART bypass mode. PIO Lines need to be pulled-up through 2.2K



3.4 PCM

Pulse Code Modulation (PCM) is a standard method used to digitize audio (particularly voice) patterns for transmission over digital communication channels. Through its PCM interface, this module has hardware support for continual transmission and reception of PCM data, so reducing processor overhead for wireless headset applications. This module offers a bi-directional digital audio interface that route directly into the baseband lauer of the on-chip firmware. It dose not pass through the HCI protocol layer.

Hardware allows the data to be sent to and received from a SCO connection. This module interfaces directly to PCM audio devices including the following:

- Qualcomm MSM 3000 series and MSM 5000 series CDMA baseband devices
- OKI MSM7705 for channel A-law and u-law CODEC
- Motorola MC145481 8-bit A-law and u-law CODEC
- Motorola MC145483 13-bit linear CODEC
- STW 5093 and 5094 14-bit linear CODECs

3.4.1 PCM Configuration

The PCM configuration is set using two PS keys, PSKEY_PCM_CONFIG32 and PSKEY_PCM_LOW_JITTER_CONFIG. The default for long frame sync and interface master generating 256KHz PCM_CLK with no tristating of PCM_OUT.

Parameter	Possible value
Mode	Slave, Master
Clock rate	Master Mode : 128, 256, 512KHz Slave Mode : up to 2048KHz
Sync formats	Long frame sync, Short frame sync
Data formats	13 or 16bit linear, 8-bit A-law to u-law

4. Boot Interface configures

The firmware configures itself when it boots by reading the value on a set PIO pins

Pin Values			Host Transport	Features	
PIO[0]	PIO[1]	PIO[4]		System Clock	Baud Rate
0	0	0	BCSP (default)	Available	Available
0	0	1	BCSP with UART configured to use 2 stop bits and no parity	Available	Available
0	1	1	USB, 26MHz crystal	Not available	Not available
1	0	0	Three-wire UART	Available	Available
1	0	1	H4DS	Available	Available
1	1	0	UART (H4)	Available	Available
1	1	1	Reserved		

6. Revision History

Revision	Date	Change Descriptions	Issued by
Rev 1.0	2005-12-27	Initial release	Narsen
Rev 1.1	2006-04-21	Size change	Narsen
Rev 1.2	2006-06-24	26 Pin Function has been modified (GND→Xtal IN/NC)	Narsen
Rev 1.3	2006-12-04	Package Change (Mold → No Mold) Size Change (Height : 1.3mm → 1.06mm)	Narsen
Rev 1.4	2011-03-09	Operating Temperature Update	J.M.Kwon